AMENDMENTS

IN THE CLAIMS:

Claim 1. (Previously Amended) A semiconductor device having:

terminal electrodes located, in plan view, outside a region where semiconductor chips are located;

a lower semiconductor chip overlapping in height with said terminal electrodes;

an upper semiconductor chip located opposite said lower semiconductor chip;

wires connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said wires, wherein said encapsulating resin and said terminal electrodes have respective bottom surfaces coplanar with each other.

Claim 2. (Previously Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and coplanar with said terminal electrodes, and wherein said lower semiconductor chip does not overlap, in plan view, said die pad.

Claim 3. (Previously Amended) The semiconductor device according to claim 1, wherein said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar with each other and the bottom surface of said lower semiconductor chip is exposed and not covered by said encapsulating resin.

Claim 4. (Previously Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and not coplanar with said terminal electrodes, and wherein said lower semiconductor chip has a bottom surface encapsulated by said encapsulating resin.

Claim 5. (Previously Amended) The semiconductor device according to claim 1, wherein said semiconductor device is a QFN (Quad Flat Non-Lead) Package having said terminal electrodes surrounding said upper and lower semiconductor chips.

Claim 6. (Previously Amended) The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are respectively rectangular in shape, connection terminals of said upper and lower semiconductor chips are arranged along shorter sides of said upper and lower semiconductor chips, opposing each other, and said upper and lower semiconductor chips cross each other, in plan view.

Claim 7. (Previously Amended) The semiconductor device according to claim 1, wherein said terminal electrodes are leads located along two opposing sides of said semiconductor device with said upper and lower semiconductor chips therebetween.

Claim 8. (Previously Amended) A semiconductor device TSOP (Thin Small Outline) Package having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of said semiconductor device, in plan view;

a first die pad integrated with and not coplanar with said first lead portion and located on one side of a reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and

a second die pad integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor chip is supported by said first die pad and said upper semiconductor chip is supported by said second die pad portion, said upper and lower semiconductor chips are partially overlapping and overlap in height with said first and second lead portions.

Claim 9. (Previously Amended) The semiconductor device according to claim 8, including:

a first lead frame connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and

a second lead frame connected to said first die pad and located, with said second lead portion, on the second side of said reference plane.

Claim 10. (Previously Amended) The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad , is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion,

said first extension and said first opposing portion have bottom surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have upper surfaces supporting said upper semiconductor chip.

Claim 11. (Previously Amended) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pads are integrated into a common lead frame, said reference plane passes centrally through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

Claim 12. (Previously Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

Claims 13-15 (Withdrawn)